@001

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. ___200209082-1___

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):   Samuel H. DUNCAN et al.

Application No.: 10/662,782

Filing Date: 09/15/2003

Confirmation No.: 1497

Examiner: J. S. Cerullo

Group Art Unit: 2112

Title: **METHOD AND SYSTEM OF COMPLETING PENDING I/O DEVICE READS IN A MULTIPLE-PROCESSOR COMPUTER SYSTEM**

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on ___03/24/2006___ .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120   ☐ 2nd Month $450   ☐ 3rd Month $1020   ☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of ___$ 500___ . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Commissioner for Patents, Alexandria, VA 22313-1450

Date of Deposit:

OR

☒ I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571)273-8300.

Date of facsimile: 04/21/2006

Typed Name: Mark E. Scott

Signature:

Number of pages: 21

Rev 10/05 (AplBrief)

Respectfully submitted,

Samuel H. DUNCAN et al.

By

Mark E. Scott

Attorney/Agent for Applicant(s)

Reg No. :   43,100

Date :   04/21/2006

Telephone :   (713) 238-8000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Samuel H. DUNCAN et al.	§	Confirmation No.:	1497
		§		
Serial No.:	10/662,782	§	Group Art Unit:	2112
		§		
Filed:	09/15/2003	§	Examiner:	Jeremy S. Cerullo
		§		
For:	Method And System Of	§	Docket No.:	200209082-1
	Completing Pending I/O	§		
	Device Reads In A	§		
	Multiple-Processor	§		
	Computer System	§		

APPEAL BRIEF

Mail Stop Appeal Brief – Patents   Date: April 21, 2006
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

    Appellants hereby submit this Appeal Brief in connection with the above-
identified application.   A Notice of Appeal was filed via facsimile on
March 24, 2006.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

TABLE OF CONTENTS

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

I.　　REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). The Assignment from the Inventors to HPDC was recorded on September 15, 2003, at Reel/Frame 014509/0848.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

II.   **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any related appeals or interferences.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

III.   **STATUS OF THE CLAIMS**

Originally filed claims:	1-22.
Claim cancellations:	15.
Added claims:	None.
Presently pending claims:	1-14 and 16-22.
Presently appealed claims:	1-4, 8 and 19.
Presently allowed claims:	5-7, 9-14, 16-18 and 20-22

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

IV.   STATUS OF THE AMENDMENTS

No claims were amended after the final Office action dated
January 24, 2006.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

V.   SUMMARY OF THE CLAIMED SUBJECT MATTER

The specification is directed to a method and system of completing pending input/output device reads in a multiple-processor computer system.[1] At least some of the illustrative embodiments are methods comprising periodically stalling issuance of input/output (I/O) device accesses by a program in a multiple-processor computer system,[2] and during the stalling step completing pending I/O device reads.[3]

Other embodiments are methods comprising periodically stalling issuance of input/output (I/O) device accesses by a program in a multiple-processor computer system,[4] and during the stalling step completing pending I/O device reads.[5] Stalling further comprises entering an interrupt mode by each processor in the multiple-processor system.[6] Entering an interrupt mode further comprises entering the interrupt mode by each of the processors substantially simultaneously.[7]

Yet still illustrative embodiments are computer systems comprising a plurality of processors coupled to each other,[8] and at least one of the plurality of processors coupled to an input/output (I/O) device by way of a bridge logic device.[9] Each of the plurality of processors periodically executes a program that

---

[1] Specification Title.

[2] Specification, Paragraph [0025], lines 12-13; Figure 3. Citations to the specification from this point forward take the form ([paragraph], lines); thus, this illustrative cite in the shorthand notation takes the form ([0025], lines 12-13).

[3] ([0026], lines 4-7); Figure 3.

[4] Specification, Paragraph [0025], lines 12-13; Figure 3. Citations to the specification from this point forward take the form ([paragraph], lines); thus, this illustrative cite in the shorthand notation takes the form ([0025], lines 12-13).

[5] ([0026], lines 4-7); Figure 3.

[6] ([0025], lines 10-12).

[7] Id.

[8] ([0012], lines 1-4); Figure 1.

[9] ([0014], lines 1-10); Figure 1.

operates to cease issuance of I/O device writes until pending I/O device reads complete.[10]

Finally, yet still other illustrative embodiments are computer systems comprising a plurality of means for executing[11] programs and instructions coupled to each other[12] (each of the plurality of means for executing coupled to a means for storing data and instructions local each of the plurality of means for executing)[13], and at least one of the plurality of means for executing coupled to a means for receiving data[14] from devices external to the computer system and for sending data to device external to the computer system[15] (the means for receiving coupled to the at least one plurality of means for executing by way of a means for bridging a first and second communication bus).[16] Each of the plurality of means for executing periodically executes programs that operate to cease issuance of writes to the means for receiving until pending writes to the means for receiving complete.[17]

---

[10] ([0025], lines 1-2); ([0025], lines 12-13); ([0026], lines 4-7); Figure 3.

[11] This limitation is specifically identified as a means plus function limitation under 35 USC 112, Sixth Paragraph.

[12] ([0012], lines 1-4); Figure 1.

[13] ([0013], lines 1-3); ([0019], lines 1-7); Figures 1 and 2.

[14] This limitation is specifically identified as a means plus function limitation under 35 USC 112, Sixth Paragraph.

[15] ([0014], lines 9-10); Figures 1 and 2.

[16] ([0014], lines 1-9); Figures 1 and 2.

[17] ([0025], lines 1-2); ([0025], lines 12-13); ([0026], lines 4-7); Figure 3.

VI.   GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1–4, 8 and 19 are anticipated by Morrison et al. (U.S. Pat. No. 6,625,679, hereinafter just "Morrison").

VII.   ARGUMENT

A.   Claims 1, 2, 4, 8 and 19

Claims 1, 2, 4, 8 and 19 stand rejected as allegedly anticipated by Morrison. Claim 8 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 USC § 282 shall apply to each of these claims individually.

Morrison is directed to an apparatus and method for converting interrupt transactions to interrupt signals to distribute interrupts to IA-32 processors.[18] In particular, Morrison describes a bridge device 112_i, coupled to plurality of processors, that collects interrupts and forward each interrupt to the appropriate processor.[19]

> The bridge 112_i that is connected to the same processor bus 114_i as the destination IA-32 processor 120_i recognizes the interrupt transaction, and asserts an interrupt pin at the targeted IA-32 processor 120_i. Since more than one interrupt could be delivered to a node, the bridge 112_i may buffer, prioritize, or throttle the interrupt transactions.[20]

As illustrated by Morrison's Figure 5, each processor to which the bridge 112 couples has its own set of registers to control buffering of interrupts.

> A set of the above registers 202-206 is supplied **for each of the IA-32 processors** 120_i handled by the bridge 112_i. **Each set 202-206 is mutually exclusive and drives one of the local LINT* lines to an IA-32 processor** 120_i.[21]

It follows that any delay in providing the particular interrupted processor the interrupt vector is on a per-processor basis.

> After asserting the INTR, the IA-32 processor 120i (eventually) generates an INTA transaction to gain access to the

---

[18] Morrison Title.

[19] Morrison Col. 3, lines 63-65; Figure 3.

[20] Morrison Col. 4, lines 13-19.

[21] Morrison Col. 7, lines 16-22 (emphasis added).

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

interrupt vector. **The bridge 112₁ responds to the INTA transaction
with the vector of the highest priority pending interrupt** at a time
after the INTA transaction was received **and after all system bus
transactions are complete that were pending prior to the
original interrupt transaction on the system bus 110.**[22]

Stated otherwise, there does not appear to be any teaching or suggestion in Morrison that there should be any delay with respect to interrupt vector delivery to the other processors, or even that the other processors have had interrupts assert to them.

Claim 8, by contrast, specifically recites, "a plurality of processors coupled to each other; at least one of the plurality of processors coupled to an input/output (I/O) device by way of a bridge logic device; and wherein each of the plurality of processors periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device reads complete." As Applicants understand Morrison, the delay to allow "system bus transactions" to complete is only with respect to a particular processor. Thus, Morrison fails to expressly or inherently teach, "wherein **each of the plurality of processors** periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device complete."

Based on the foregoing, Appellants respectfully submit that the rejections of the claims in this first grouping be reversed, and the claims set for issue.

B.   Claim 3

Claims 3 stands rejected as allegedly anticipated by Morrison.

Claim 3 specifically recites, "wherein entering the interrupt mode further comprises entering the interrupt mode by each of the processors substantially simultaneously." Morrison fails to expressly or inherently teach any coordination in the timing of entering any interrupt mode as between the processor.

Based on the foregoing, Appellants respectfully submit that the rejections of the claim in this second grouping be reversed, and the claim set for issue.
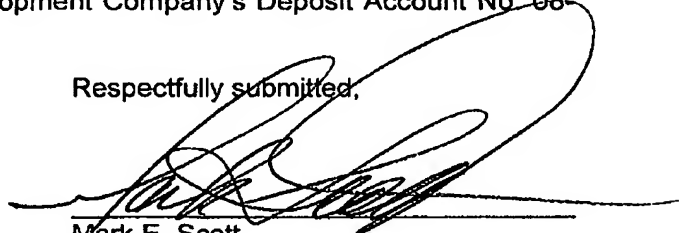
_____

[22] Morrison Col. 7, lines 30-37 (emphasis added).

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

C.   Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

Mark E. Scott
PTO Reg. No. 43,100
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPELLANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

VIII.   CLAIMS APPENDIX

1.   (Original) A method comprising:

periodically stalling issuance of input/output (I/O) device accesses by a
program in a multiple-processor computer system; and during the
stalling step

completing pending I/O device reads.

2.   (Original) The method as defined in claim 1 wherein periodically stalling
further comprises entering an interrupt mode by each processor in the multiple-
processor system.

3.   (Original) The method as defined in claim 2 wherein entering an interrupt
mode further comprises entering the interrupt mode by each of the processors
substantially simultaneously.

4.   (Original) The method as defined in claim 1 wherein after completing
pending I/O device reads, the method further comprises allowing each processor
in the multiple-processor to resume issuing I/O device accesses.

5.   (Previously presented) A method comprising:

periodically stalling issuance of input/output (I/O) device accesses by a
program in a multiple-processor computer system;

completing pending I/O device reads during the stalling issuance of I/O
device accesses; and then

allowing each processor in the multiple-processor to resume issuing I/O
device accesses by asserting a resume flag associated within each
processor by a processor designated as primary.

6.   (Original) The method as defined in claim 5 wherein asserting a resume
flag further comprises asserting a resume flag in a port logic of each of the
processors.

7.   (Original) The method as defined in claim 5 wherein asserting a resume flag further comprises asserting a resume flag in a read/write portion of a memory coupled to each of the processors.

8.   (Original) A computer system comprising:
        a plurality of processors coupled to each other;
        at least one of the plurality of processors coupled to an input/output (I/O)
                device by way of a bridge logic device; and
        wherein each of the plurality of processors periodically executes a program
                that operates to cease issuance of I/O device writes until pending
                I/O device reads complete.

9.   (Previously presented) A computer system comprising:
        a plurality of processors coupled to each other;
        at least one of the plurality of processors coupled to an input/output (I/O)
                device by way of a bridge logic device;
        a plurality of flag registers associated one each with the plurality of
                processors; and
        wherein each of the plurality of processors periodically executes a program
                that operates to cease issuance of I/O device writes until pending
                I/O device reads complete, and wherein at least some of the
                plurality of processors resume issuance of I/O device writes upon
                assertion of their associated flag registers.

10.   (Original) The computer system as defined in claim 9 wherein each flag register is external to each processor.

11.   (Original) The computer system as defined in claim 10 further comprising:
        a plurality of memory devices coupled one each to at least some of the
                plurality of processors;
        wherein each flag register is in a local memory of each processor.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

12.   (Original) The computer system as defined in claim 9 wherein each flag register is internal to each processor.

13.   (Original) The computer system as defined in claim 12 wherein each processor further comprises a port logic, and wherein the flag register is located within the port logic.

14.   (Previously presented) A method comprising:
        a plurality of processors coupled to each other one of the plurality of processors designated a primary processor; and
        at least one of the plurality of processors coupled to an input/output (I/O) device by way of a bridge logic device;
        wherein each of the plurality of processors periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device reads complete; and
        wherein the primary processor is programmed to issue a read to the bridge logic device after cessation of I/O device writes, and wherein when the read to the bridge device completes the primary processor is further programmed to allow the computer system to resume issuance of I/O device writes.

15.   (Cancelled).

16.   (Previously presented) A processor comprising:
        a core region;
        a memory controller; and
        a port logic coupled to the core region and the memory controller, the port logic comprising a register;
        wherein the processor periodically enters an interrupt mode, and during the interrupt mode the processor executes firmware that operates to stop production of input/output (I/O) device write requests, and wherein the

processor exits the interrupt mode and resumes production of I/O device writes when the register is asserted.

17.   (Previously presented) A processor comprising:

a core region;

a memory controller; and

a port logic coupled to the core region and the memory controller, wherein
the processor couples to one or more bus bridges by way of the
port logic;

wherein the processor periodically enters an interrupt mode, and during
the interrupt mode the processor executes firmware that operates to
stop production of input/output (I/O) device write requests; and

wherein during the interrupt mode the processor issues read commands to
each of the one or more bus bridges if the processor has a primary
designation.

18.   (Original) The processor as defined in claim 17 wherein during the interrupt mode the processor commands other processors to resume production of I/O device write requests if the processor has a primary designation.

19.   (Previously presented) A computer system comprising:

a plurality of means for executing programs and instructions coupled to
each other, each of the plurality of means for executing coupled to a
means for storing data and instructions local each of the plurality of
means for executing:

at least one of the plurality of means for executing coupled to a means for
receiving data from devices external to the computer system and for
sending data to device external to the computer system, the means
for receiving coupled to the at least one plurality of means for
executing by way of a means for bridging a first and second
communication bus; and

wherein each of the plurality of means for executing periodically executes programs that operate to cease issuance of writes to the means for receiving until pending writes to the means for receiving complete.

20.   (Previously presented) A computer system comprising:

a plurality of means for executing programs and instructions coupled to each other, each of the plurality of means for executing coupled to a means for storing data and instructions local each of the plurality of means for executing;

at least one of the plurality of means for executing coupled to a means for receiving data from devices external to the computer system and for sending data to device external to the computer system, the means for receiving coupled to the at least one plurality of means for executing by way of a means for bridging a first and second communication bus; and

a plurality of means for triggering associated one each with the plurality of means for executing;

wherein each of the plurality of means for executing periodically executes programs that operate to cease issuance of writes to the means for receiving until pending writes to the means for receiving complete; and

wherein at least some of the plurality of means for executing resume issuance of writes to the means for receiving upon assertion of their associated means for triggering.

21.   (Original) The computer system as defined in claim 20 wherein each means for triggering is in the means for storing coupled to each means for executing.

22.   (Original) The computer system as defined in claim 20 wherein each means for triggering is in its associated means for executing.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

IX.   EVIDENCE APPENDIX

None.

Appl. No. 10/662,782
Appeal Brief dated April 21, 2006
Reply to final Office action of January 24, 2006

X.   RELATED PROCEEDINGS APPENDIX

None.